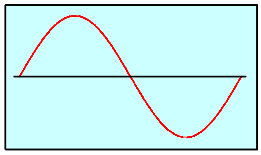

Professional Audio Creativity

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This circuit gives full details necessary to build a four band parametric equaliser, with high-pass filter, balanced input and output.
Hopefully, the following notes will enable anyone to make any necessary changes to suit their individual requirements.

Equaliser Circuitry

Some compromises have been made with the design, mainly in order to avoid the requirement for pots with obscure laws. Although pots with, for example, 47k reverse log tracks, are available, they are probably not as widely obtainable as those with 10k linear tracks, so unless otherwise noted, all pots have 10k linear tracks. The amplitude pots do require to have a centre tap, which is grounded. If untapped pots are used, the sections will interact quite severely, and the constant Q characteristic will be lost.
Due to the use of linear pots, the frequency controls of the high and low shelving filters do not track the associated state variable sections particularly well. If reverse log pots are used for the frequency controls, they should be wired in series with the resistors feeding the integrators, and the resistors to ground omitted. The integrator capacitors will need to be re-calculated, and the shelving filters will use the same values as the state-variables.
The circuit as drawn, has approximately 10dB of lift and cut. This is set by the value of the resistors feeding the wipers of the amplitude pots – 2k2 in this case. For other amounts of lift and cut, these resistors need to be changed to the following values:

Amplitude	Change Resistor to:	Actual Amplitude
6dB	5k1	6.02dB
8dB	3k3	8.12dB
10dB	2k2	10.42dB
12dB	1k6	12.44dB
15dB	1k1	15.02dB
18dB	750R	17.84dB

The frequency calculations are slightly more complicated – the maximum frequency of each band is set by the capacitors of the respective state variable filter, combined with the resistors between the pot wipers and the inverting inputs of the integrator stages. Taking the 400Hz to 4kHz section as an example, these are 10nF and 3k9. Using the formula $1/(2*\pi*R*C)$ this gives a frequency of 4081Hz. At the other end of the potentiometer travel, it is easier to work out the value of the limiting resistor by using a simulation programme, and this is the method I employed throughout.
The range of “Q” values (1 to 3) is about optimum, as to increase the range would be at the expense of noise, but anyone needing to experiment should try adjusting the

values of the 10k input, 5k1 feedback and 4k7 pot standoff resistors. Keep in mind that any changes made to the 10k and 5k1 values, must be reflected by similar values being used for the feedback and input resistors of the inverting amplifier that is the output stage of the state variable network.

Input Stage

Note that the input signal has been attenuated by 6dB in order to increase the headroom to 28dB above 0dBu. Provision has been made for the input amplifier to have gain, in case the unit is required to work with domestic equipment. If this is not the case, R20 should be omitted, and R6 and R7 should be 10R. If input gain is required, R21 should be omitted and both R5 and R8 reduced to 1k. The value of R6 and R7 should be increased to 4k7, and R20 is then calculated from the formula:

(R6+R7)/(Alog(G/20)-1)

As an example, if the gain required (G) is 10dB, R20 should be 4k3 (or 4k347 to be precise) The result can be checked by the gain formula:

G(dB)=20*log(((R6+R7)/R20)+1)

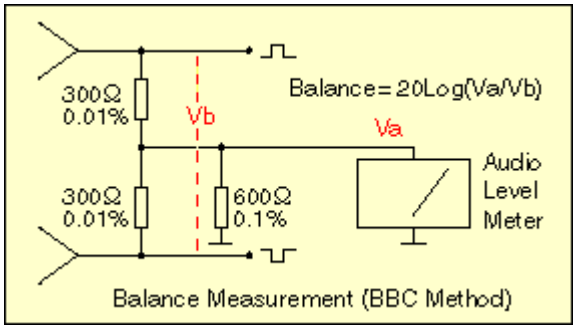
The input common mode rejection is set in the following manner:
Apply a 100Hz signal to the input, and monitor the output of the stage at the top of R11 using either an oscilloscope or AC meter capable of reading down to –80dBu. Set the input signal level so that it is at +20dBu (7.75V) at the top of R11. Now join the two inputs together and apply the same signal to the junction. Adjust P1 for *minimum* signal at the top of R11. Change the input signal frequency to 10kHz and adjust C36 for minimum output. Repeat these steps two or three times to reduce interaction between the two controls. With careful adjustment, a common mode rejection ratio of 60 or 70dB should be attainable.

Output Stage

The output amplifier has an inherent gain of 6dB, but this can be increased by utilizing R26 and R27. Normally, R27 will be 10R with R26 omitted, but to increase the output gain, R27 should be 4k7 and the value of R8 calculated from:

R27/(Alog(G/20)-1)

Again, as an example, if an additional 10dB of output gain is required, R26 would be 2k2 (or 2k174 if you happen to have one in your resistor collection)
Output balance is adjusted in the following manner:



Set the output level to +20dBu, and measure the level at the junction of the two 300R resistors. (These do not have to be precisely 300R, but they must be matched to within 0.01%) Adjust P2 for *minimum* signal at the junction, then change the input signal frequency to 10kHz and adjust C41, again for minimum signal. Repeat these adjustments two or three times to reduce interaction between the two controls. It should be possible to obtain a balance, over the audio bandwidth, of better than –60dB, and in some instances, -90dB may be attainable.

Note that whereas the schematic gives all the op-amps as NE5532, you may experiment with other types which have the standard pin-out

I have started doing a PCB layout of this circuit, but as I can only justify working on it in my spare time, it may be a while before it appears. It will be double sided with PTH and a ground plane connected to 0V on both sides. I will publish it in Gerber format so anyone can get their own PCB's made.
There is one problem concerning the component footprints used, particularly the potentiometers, as the only ones in my library are not readily available (unless you order a couple of thousand) so I would suggest panel mounting an available type and wiring these to pins on the PCB. I think all the other components are available from either Farnell or R-S Components, and when I get time I will generate a parts list with the relative stock numbers listed.
The only other small problem is that when the PCB is complete, the components will be re-numbered on the schematic. At that time, I will post a new schematic that is in agreement with the PCB, and also change the references in this note.

Watch this space….

Still watching? Well, the PCB is done, and the Gerber files are the reason this zip file has grown somewhat. It's not the greatest layout in the World, as it was done in rather a hurry, but it should work without too many problems. I've included both a .pdf of the PCB tracking, and a GC-Prevue file you can play with. (You can download a free copy of GC-Prevue from www.graphicode.com if you want to have a play with the Gerber files – I have version 9 which is fine)

I hope I haven't made any mistakes – no doubt someone will soon shout if I have (If that someone is Martin Griffith, he knows where he can go!)

Best wishes

Barry E Porter
April 2001